12. [Amended] The transistor of claim [11] 28, wherein materials comprising at least one of the floating gate and the insulator are selected to have an electron affinity causing the barrier energy to be selected at less than approximately 3.3 eV.

13. [Four times amended] The transistor of claim 28, wherein:

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

the barrier energy is less than approximately 2.0 eV; and

an area of a capacitor formed by the control electrode, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

19. [Three times amended] A transistor comprising:

a source region;

a drain region;

a channel region between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and [wherein] a barrier energy between the floating gate and the insulator [is] being less than approximately [3.3] 2.0 eV;

a control electrode, separated from the floating gate by an intergate dielectric; and

wherein the intergate dielectric has a permittivity that is higher than a permittivity of silicon dioxide.

28. [Amended] A transistor comprising:

a source region;

a drain region;

a channel region between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate

comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV;

a control electrode, separated from the floating gate by an intergate dielectric; and

wherein the intergate diclectric has a permittivity that is higher than a permittivity of silicon dioxide.

29. [Three Times Amended] A memory cell comprising:

a storage electrode comprising a material that has a smaller electron affinity than polycrystalline silicon to store chargc;

an insulator adjacent to the storage electrodc, wherein a barrier energy between the insulator and the storage electrode is less than approximately 3.3 cV;

a control electrode separated from the storage clectrodc by an intcrgate dielectric; and

wherein the intergate dielectric has a permittivity that is higher than a permittivity of silicon dioxidc.

32. [Twice Amended] A memory device comprising:

a plurality of mcmory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channcl rcgion between the source and drain regions;

a floating gate separated from the channel rcgion by an insulator, the floating gatc comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximatcly 3.3 eV; and

a control gatc located adjacent to the floating gate and scparated therefrom by an intergate dielectric having a pcrmittivity that is higher than a permittivity of silicon dioxide.

21. 34. [Amended] The memory device of claim [33] 32 wherein materials comprising at least one of the floating gate and the insulator in each transistor are selected to have an electron affinity causing the barrier energy to be less than approximately 3.3 eV.

E9

23. 36. [Amended] The memory device of claim [33] 32 wherein the floating gate of each transistor is isolated from conductors and semiconductors.

E10 24. 37. [Amended] The memory device of claim [33] 32 wherein the insulator in each transistor comprises a material that has a larger electron affinity than silicon dioxide.

25. 38. [Twice amended] The memory device of claim 32 wherein:

E11 the insulator comprises a material that has a larger electron affinity than silicon dioxide;

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

the barrier energy is less than approximately 2.0 eV; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region of each transistor.

19. 41. [Amended] The transistor of claim 18 wherein:

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

[the floating gate comprises a material that has a smaller electron affinity than polycrystalline silicon;]

E12 an area of a capacitor formed by the control electrode, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region[; and

the barrier energy is less than approximately 2.0 eV].

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42. [Amended] The memory cell of claim 2~~9~~, further comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region; and wherein:

the storage electrode comprises polycrystalline or microcrystalline silicon carbide;

[an] the insulator is between the storage electrode and the channel region, the insulator comprising a material that has a larger electron affinity than silicon dioxide, [and a] and the barrier energy [between the insulator and the storage electrode being] is less than approximately [3.3] 2.0 eV; and

[wherein the storage electrode comprises a material that has a smaller electron affinity than polycrystalline silicon; and]

[wherein] an area of a capacitor formed by the control electrode, the storage electrode, and the intergate dielectric is larger than an area of a capacitor formed by the storage electrode, the insulator, and the channel region.

cont.

E1228.

43. [Amended] A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

an insulator comprising a material that has a larger electron affinity than silicon dioxide;

a floating gate separated from the channel region by the insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and

a control gate, separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

29. 44. [Amended] The transistor of claim 43 28 wherein:

the insulator comprises amorphous silicon carbide;

the floating gate comprises [a material that has a smaller electron affinity than polycrystalline silicon] polycrystalline or microcrystalline silicon carbide;

cont. an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and E12

the barrier energy is less than approximately 2.0 eV.

32. 47. [Amended] A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV;

a control gate, separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide; and

wherein an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region. E13

33. 48. [Amended] The transistor of claim 47 32 wherein:

the floating gate comprises [a material that has a smaller electron affinity than polycrystalline silicon] polycrystalline or microcrystalline silicon carbide;

the insulator comprises a material that has a larger electron affinity than silicon dioxide; and

the barrier energy is less than approximately 2.0 eV.

37.
49. [Amended] A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

an insulator comprising a material that has a larger electron affinity than silicon dioxide;

a floating gate separated from the channel region by the insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; [and]

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide[.]; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

35. 34
50. [Amended] The transistor of claim 49 wherein:

cont.

the insulator comprises amorphous silicon carbide;

E13

the [a] barrier energy [between the floating gate and the insulator] is less than approximately [3.3] 2.0 eV; and

the floating gate comprises polycrystalline or microcrystalline silicon carbide. [a material that has a smaller electron affinity than polycrystalline silicon; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.]

36.
51. [Amended] A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate

comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

37. 52. [Amended] The transistor of claim 36 51 wherein:

[a] the barrier energy [between the floating gate and the insulator] is less than approximately [3.3] 2.0 eV;

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

the insulator comprises a material that has a larger electron affinity than silicon dioxide; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

cont. 38. E13 54. [Amended] A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 2.0 eV;

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide; and

wherein an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

39. 54. [Amended] The transistor of claim 38 wherein:

[a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;]

the insulator comprises a material that has a larger electron affinity than silicon dioxide; and

the floating gate comprises [a material that has a smaller electron affinity than polycrystalline silicon] polycrystalline or microcrystalline silicon carbide.

40. 55. [Amended] A memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

an insulator comprising a material that has a larger electron affinity than silicon dioxide;

a floating gate separated from the channel region by the insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and

cont. E13

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

41. 56. [Amended] The memory cell of claim 55 wherein:

the insulator comprises amorphous silicon carbide;

[a] the barrier energy [between the floating gate and the insulator] is less than approximately [3.3] 2.0 eV;

the floating gate comprises [a material that has a smaller electron affinity than polycrystalline silicon] polycrystalline or microcrystalline silicon carbide; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

42.
57. [Amended] A memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

43. 42
58. [Amended] The memory cell of claim 57 wherein:

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

cont. [a] the barrier energy [between the floating gate and the insulator] is less than approximately [3.3] 2.0 eV;

E13 the insulator comprises a material that has a larger electron affinity than silicon dioxide; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

44.
59. [Amended] A memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV;

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide; and

wherein an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

45. 60. [Amended] The memory cell of claim 44 wherein:

[a] the barrier energy [between the floating gate and the insulator] is less than approximately [3.3] 2.0 eV;

the insulator comprises a material that has a larger electron affinity than silicon dioxide; and

the floating gate comprises [a material that has a smaller electron affinity than polycrystalline silicon] polycrystalline or microcrystalline silicon carbide.

cont. 46. 61. [Amended] A memory cell comprising:

E13

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately [3.3] 2.0 eV; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

47. 62. [Amended] The memory cell of claim 46 wherein:

[the barrier energy is less than approximately 2.0 eV;]

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

the floating gate comprises [a material that has a smaller electron affinity than polycrystalline silicon] polycrystalline or microcrystalline silicon carbide; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate

dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

48.
63. [Amended] A memory device comprising:

a plurality of memory cells, each memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

an insulator comprising a material that has a larger electron affinity than silicon dioxide;

a floating gate separated from the channel region by the insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

cont.
E13 49.
64. [Amended] The memory device of claim 63 48 wherein:

the insulator comprises amorphous silicon carbide;

[a] the barrier energy [between the floating gate and the insulator] is less than approximately [3.3] 2.0 eV;

the floating gate comprises [a material that has a smaller electron affinity than polycrystalline silicon] polycrystalline or microcrystalline silicon carbide;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

50.

65. [Amended] A memory device comprising:

a plurality of memory cells, each memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

cont.

a channel region in the substrate between the source region and the drain region;

E13

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

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51. 50

66. [Twice amended] The memory device of claim 65 wherein:

the barrier energy [between the floating gate and the insulator] is less than approximately 2.0 eV;

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

the floating gate comprises [a material that has a smaller electron affinity than polycrystalline silicon] polycrystalline or microcrystalline silicon carbide;

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an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

52.
67. [Amended] A memory device comprising:

a plurality of memory cells, each memory cell comprising:

a source region in a substrate;

cont. a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

E14 a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 2.0 eV; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

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53. 52
68. [Twice amended] The memory device of claim 67 wherein:

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

[a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;]

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

an area of a capacitor formed by the control gate, the floating gate, and the intergate

E15 dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

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54 69. [Amended] A memory device comprising:

a plurality of memory cells, each memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV;

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a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide; and

wherein an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

55. 54 70. [Twice amended] The memory device of claim 69 wherein:

[a] the barrier energy [between the floating gate and the insulator] is less than approximately [3.3] 2.0 eV;

the floating gate comprises [a material that has a smaller electron affinity than polycrystalline silicon] polycrystalline or microcrystalline silicon carbide;

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

E17 and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

60. [Amended] The memory device of claim 39 wherein:

the barrier energy is less than approximately 2.0 eV;

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

E 18

61. [Amended] A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV, the floating gate being capacitively separated from the channel region to provide transconductance gain; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

62. 61
78. [Amended] The memory device of claim 77 wherein:

the floating gate comprises polycrystalline or microcrystalline silicon carbide [and has a smaller electron affinity than polycrystalline silicon];

[a] the barrier energy [between the floating gate and the insulator] is less than approximately [3.3] 2.0 eV;

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

cont.

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the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.